REMARKS

Receipt of the Office Action of June 4, 2007 is hereby acknowledged. In that action the Examiner: 1) rejected claims 9-20 as allegedly unpatentable over McGrath et al. (U.S. Pat. No. 6,973,562, hereinafter McGrath); 2) rejected claims 1, 5-6, 8 and 21-33 as allegedly unpatentable over McGrath in view of Tran (U.S. Pat. No. 6,367,006); and 3) rejected claims 2-4 and 7 as allegedly unpatentable over McGrath, Tran and Seal et al. (U.S. Pat. No. 6,965,984).

With this Response, Applicants amend claim 9 and present new claim 34.

I. ART-BASED REJECTIONS

A. Claim 1

Claim 1 stands rejected as allegedly obvious over McGrath and Tran.

McGrath is directed to establishing an operating mode in a processor. (McGrath Title). In particular, McGrath discloses a processor having different operating modes **that establish the address size and operand size** for instructions executed by the processor.

> [T]he operating mode may specify a default operand size and a default address size. The default operand size specifies the number of bits in an operand of an instruction… . The default address size specifies the number of bits in an address of a memory operand of an instruction… .

(McGrath Col. 3, line 66 – Col. 4, line 6). The instruction set the processor executes remains the same, but the operating mode sets the size of the operands for each instruction.

> More particularly, execution core 14 fetches operands having the default operand size … unless a particular instruction's encoding overrides the default operand size, in which case the overriding operand size is used. Similarly, execution core 14 generates addresses of memory operands, wherein the addresses have the default address size unless a particular instruction's encoding overrides the default address size, in which case the overriding address size is used.

(McGrath Col. 4, lines 29-41). Similarly for the instructions themselves, the instruction set remains the same, but the addresses used to identify the location of each instruction in memory are different in each operating mode of the processor. (McGrath Col. 4, lines 46-

67). As further evidence that a single instruction set is used, reference is made to the Intel® 64 and IA-32 Architectures Software Developer's Manual (Volumes 2A and 2B) – Instruction Set Reference. (*See, e.g.*, http://www.intel.com/design/processor/manuals/253666.pdf (Volume 2A, page 3-33), the ADC (add with carry) instruction opcode 15 is operable both in the 64, 32 and legacy 16 modes)).

Claim 1, by contrast, specifically recites, "decode logic configured to decode instructions from a first instruction set in a first mode and configured to decode instructions from a second instruction set in a second mode, wherein the decode logic is configured to switch from one mode to another temporarily or for a plurality of instructions." Applicants respectfully submit that McGrath and Tran fail to teach or suggest such a processor. In particular, the McGrath processor only operates on a single instruction set. The modes of operation of the McGrath processor change only the bit-width of the operands upon which the instructions operate, or the number of bits in the address that identifies an instruction. Applicants respectfully submit that a change in the way a particular instruction in memory is addressed is not a change of instruction set for the instruction. Likewise, a change in the number of bits upon which an instruction operates is not a change of instruction set for the instruction. Thus, even if the teachings of Tran are precisely as the Office action suggests (which Applicants do not admit), McGrath and Tran still fail to teach "decode logic configured to decode instructions **from a first instruction set** in a first mode and configured to decode instructions **from a second instruction set** in a second mode."

Based on the foregoing, Applicants respectfully submit that claim 1, and all claims which depend from claim 1 (claims 2-8), should be allowed.

B. Claim 9

Claim 9 stands rejected as allegedly unpatentable over McGrath. Applicants amend claim 9 to correct a grammatical shortcoming, and not to define over any cited art.

McGrath is directed to establishing an operating mode in a processor. (McGrath Title). In particular, McGrath discloses a processor having different operating modes **that**

establish the address size and operand size for instructions executed by the processor.

> [T]he operating mode may specify a default operand size and a default address size. The default operand size specifies the number of bits in an operand of an instruction… . The default address size specifies the number of bits in an address of a memory operand of an instruction… .

(McGrath Col. 3, line 66 – Col. 4, line 6). The instruction set the processor executes remains the same, but the operating mode sets the size of the operands for each instruction.

> More particularly, execution core 14 fetches operands having the default operand size … unless a particular instruction's encoding overrides the default operand size, in which case the overriding operand size is used. Similarly, execution core 14 generates addresses of memory operands, wherein the addresses have the default address size unless a particular instruction's encoding overrides the default address size, in which case the overriding address size is used.

(McGrath Col. 4, lines 29-41). Similarly for the instructions themselves, the instruction set remains the same, but the addresses used to identify each instruction are different in each operating mode of the processor. (McGrath Col. 4, lines 46-67). As further evidence that a single instruction set is used, reference is made to the Intel® 64 and IA-32 Architectures Software Developer's Manual (Volumes 2A and 2B) – Instruction Set Reference. (*See, e.g.*, http://www.intel.com/design/processor/manuals/253666.pdf for volume 2A). As shown in the illustrative manual, a single instruction set spans 64, 32 and legacy 16 architectures.

Claim 9, by contrast, specifically recites, "decoding instructions from the first instruction set in a first mode and decoding instructions from the second instruction set in a second mode." Applicants respectfully submit that McGrath does not teach or fairly suggest such a system. McGrath clearly teaches a processor having a single instruction set, and where the operand width used by each instruction and/or the size of the virtual address space used to identify each instruction may change depending on the operating mode. Thus, McGrath fails to teach or fairly suggest "decoding instructions from **the first**

instruction set in a first mode and decoding instructions from **the second instruction set in a second mode.**" For this reason alone the rejections of claim 9 should be withdrawn and the claim set for issue.

Moreover, claim 9 recites, "the decoding of both instruction sets is performed on a single decoder." In McGrath, switching operating modes only changes the operand width upon which an instruction operates and/or the address used to identify the instruction. Thus, McGrath's decoder fails to teach or suggest a method where "the decoding of both instruction sets is performed on a single decoder."

Based on the foregoing, Applicants respectfully submits that claim 9, and all claims which depend from claim 9 (claims 10-20), should be allowed.

C. Claim 21

Claim 21 stands rejected as allegedly unpatentable over McGrath and Tran.

Claim 21, by contrast, specifically recites, "decode logic configured to decode instructions from a first instruction set in a first mode and configured to decode instructions from a second instruction set in a second mode." Applicants respectfully submit that McGrath and Tran fail to teach or suggest such a processor. In particular, the McGrath processor only operates on a single instruction set. The modes of operation of the McGrath processor change only the bit-width of the operands upon which the instructions operate, or the number of bits in the address that identifies an instruction. Applicants respectfully submit that a change in the way a particular instruction in memory is addressed is not a change of instruction set for the instruction. Likewise, a change in the number of bits upon which an instruction operates is not a change of instruction set for the instruction. Thus, even if the teachings of Tran are precisely as the Office action suggests (which Applicants do not admit), McGrath and Tran still fail to teach "decode logic configured to decode instructions from **a first instruction set in a first mode** and configured to decode instructions from **a second instruction set in a second mode**", and "wherein the processor comprises **a status register** configured to indicate whether the decode logic is decoding instructions in the **first mode** or the **second mode**".

Based on the foregoing, Applicants respectfully submit that claim 21, and all claims which depend from claim 21 (claims 22-26), should be allowed.

D. Claim 27

Claim 27 stands rejected as allegedly unpatentable over McGrath and Tran.

Claim 27, by contrast, specifically recites, "decode logic configured to decode instructions from a first instruction set in a first mode and configured to decode instructions from a second instruction set in a second mode." Applicants respectfully submit that McGrath and Tran fail to teach or suggest such a processor. In particular, the McGrath processor only operates on a single instruction set. The modes of operation of the McGrath processor change only the bit-width of the operands upon which the instructions operate, or the number of bits in the address that identifies an instruction. Applicants respectfully submit that a change in the way a particular instruction in memory is addressed is not a change of instruction set for the instruction. Likewise, a change in the number of bits upon which an instruction operates is not a change of instruction set for the instruction. Thus, even if the teachings of Tran are precisely as the Office action suggests (which Applicants do not admit), McGrath and Tran still fail to teach "decode logic configured to decode instructions from **a first instruction set in a first mode** and configured to decode instructions from **a second instruction set in a second mode**", and "wherein the system comprises **a status register** configured to indicate whether the decode logic is decoding instructions in the **first mode** or the **second mode**".

Based on the foregoing, Applicants respectfully submit that claim 27, and all claims which depend from claim 27 (claims 28-33), should be allowed.

II. NEW CLAIM

With this Response, Applicants present new claim 34, which depends from claim 21. Even if it is hypothetically considered that McGrath's instructions operating with varying address widths and/or varying operand bit-widths are different instruction sets (which Applicants do not admit), the cited art still fails to teach a decoder that decodes two instruction sets, one being stack-based and one being register-based.

III. CONCLUSION

In the course of the foregoing discussions, Applicants may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and the cited art which have yet to be raised, but which may be raised in the future.

Applicants respectfully request reconsideration and that a timely Notice of Allowance be issued in this case. If the Examiner feels that a telephone conference would expedite the resolution of this case, he is respectfully requested to contact the undersigned. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to the Texas Instruments, Inc. Deposit Account No. 20-0668.

Respectfully submitted,

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